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1	BRS	L1	51	segment adj register SAME "segment selector" SAME " segment descriptor"	USPAT; US-PGPUB; EP ; JP ; DERWENT; IBM_TDB	2004/05/10 16:17	
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5	BRS	L5	13	4 and virtual adj address	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:20	
6	BRS	L6	12	4 and virtual adj address and exception	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:21	
7	BRS	L7	12	4 and virtual adj address and exception and active and enable	USPAT; US-PGPUB; EP ; JP ; DERWENT; IBM_TDB	2004/05/10 16:22	

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8	BRS	L8	0	7 and ((update near3 (segment adj register)) near3 (load near3 instruction))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:24	
9	BRS	L9	0	7 and ((update WITH (segment adj register)) WITH (load near3 instruction))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:24	
10	BRS	L10	0	4 and ((update WITH (segment adj register)) WITH (load near3 instruction))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:25	
11	BRS	L11	5	7 and (update WITH (segment adj register))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:25	
12	BRS	L12	1	"6041403".PN.	USPAT	2004/05/10 16:30	
13	BRS	L13	1	"5850532".PN.	USPAT	2004/05/10 16:31	
14	BRS	L14	7	4 and addressing adj mode	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:42	
15	BRS	L15	2	14 not 11	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/10 16:42	

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1 ARPS: a new real-time computer
Kenneth J. Thurber
October 1976 **ACM SIGARCH Computer Architecture News**, Volume 5 Issue 4
Full text available: pdf(1.14 MB) Additional Information: full citation, references

2 Virtual machine monitors: Xen and the art of virtualization
Paul Barham, Boris Dragovic, Keir Fraser, Steven Hand, Tim Harris, Alex Ho, Rolf Neugebauer, Ian Pratt, Andrew Warfield
October 2003 **Proceedings of the nineteenth ACM symposium on Operating systems principles**
Full text available: pdf(168.76 KB) Additional Information: full citation, abstract, references, index terms

Numerous systems have been designed which use virtualization to subdivide the ample resources of a modern computer. Some require specialized hardware, or cannot support commodity operating systems. Some target 100% binary compatibility at the expense of performance. Others sacrifice security or functionality for speed. Few offer resource isolation or performance guarantees; most provide only best-effort provisioning, risking denial of service.This paper presents Xen, an x86 virtual machine monit ...

Keywords: hypervisors, paravirtualization, virtual machine monitors

3 An advanced tactical computer concept
Kenneth J. Thurber, Peter C. Patton, Robert C. Deward, Jon C. Strauss, Thomas W. Petschauer
March 1977 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th annual symposium on Computer architecture**, Volume 5 Issue 7
Full text available: pdf(432.42 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses the design of a real-time computer. The computer's design requirements, design decisions, and architecture are summarized. The paper discusses how the design requirements influenced the computer architecture. The system's three upward compatible addressing options (real, base, virtual) are also discussed.

4 Performance effects of architectural complexity in the Intel 432
Robert P. Colwell, Edward F. Gehringer, E. Douglas Jensen
August 1988 **ACM Transacti ns n Computer Systems (TOCS)**, Volume 6 Issue 3
Full text available: pdf(3.45 MB) Additional Information: full citation, abstract, references, citings, index terms

The Intel 432 is noteworthy as an architecture incorporating a large amount of functionality that most other systems perform by software. It has, in effect, "migrated" this functionality from the software into the microcode and hardware. The benefits of functional migration have recently been a subject of intense controversy, with critics claiming that a complex architecture is inherently less efficient than a simple architecture with good software support. This paper examines t ...

5 High-speed local area networks and their performance: a survey
Bandula W. Abeysundara, Ahmed E. Kamal
June 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue 2
Full text available: pdf(3.83 MB) Additional Information: full citation, abstract, references, citings, index terms, review

At high data transmission rates, the packet transmission time of a local area network (LAN) could become comparable to or less than the medium propagation delay. The performance of many LAN schemes degrades rapidly when the packet transmission time becomes small comparative to the medium propagation delay. This paper introduces LANs and discusses the performance degradation of LANs at high speeds. It surveys recently proposed LAN schemes designed to operate at high data rates, including the ...

Keywords: access schemes, computer networks, data communication, medium access protocols, optical fiber networks

6 Binary translation and architecture convergence issues for IBM system/390
Michael Gschwind, Kemal Ebcioğlu, Erik Altman, Sumedh Sathaye
May 2000 **Proceedings of the 14th international conference on Supercomputing**
Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, index terms

We describe the design issues in an implementation of the ESA/390 architecture based on binary translation to a very long instruction word (VLIW) processor. During binary translation, complex ESA/390 instructions are decomposed into instruction "primitives" which are then scheduled onto a wide-issue machine. The aim is to achieve high instruction level parallelism due to the increased scheduling and optimization opportunities which can be exploited by binary translation software ...

7 The HP 3000 computer system
Joel F. Bartlett
November 1973 **Proceedings of the ACM-IEEE symposium on High-level-language computer architecture**
Full text available: pdf(487.44 KB) Additional Information: full citation, abstract, references, citings, index terms

The HP 3000 (1) is a 16-bit multiprogramming computer. Multiprogramming is facilitated through the use of a virtual memory scheme using code and data segmentation. The impetus for this machine was HP's growth in the time sharing market. The original offering in this area was the 2000A, a BASIC system using the HP 2116. This use and real-time demands from HP's other divisions led to the 3000's development. The 2100 (2), the 2116's successor and classical one-address machine, did not readily ...

8 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science
William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young
March 1968 **Communicati ns f the ACM**, Volume 11 Issue 3
Full text available: pdf(6.63 MB) Additional Information: full citation, references, citings

Keywords: computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

9 The Apertos reflective operating system: the concept and its implementation
Yasuhiko Yokote
October 1992 **ACM SIGPLAN Notices , conference proceedings on Object-oriented programming systems, languages, and applications**, Volume 27 Issue 10
Full text available: pdf(2.58 MB) Additional Information: full citation, references, citings, index terms

10 Associative and Parallel Processors
Kenneth J. Thurber, Leon D. Wald
December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4
Full text available: pdf(2.62 MB) Additional Information: full citation, references, citings, index terms

11 Roaming and handoff management: MobileNAT: a new technique for mobility across heterogeneous address spaces
Milind Buddhikot, Adiseshu Hari, Kundan Singh, Scott Miller
September 2003 **Proceedings of the 1st ACM international workshop on Wireless mobile applications and services on WLAN hotspots**
Full text available: pdf(303.28 KB) Additional Information: full citation, abstract, references, index terms

We propose a new network layer mobility architecture called MobileNAT to efficiently support micro and macro-mobility in and across heterogeneous address spaces common in emerging public networks. The key ideas in this architecture are as follows: (1) Use of two IP addresses -- an invariant virtual IP address for host identification at the application layer and an actual routable address at the network layer that changes due to mobility. Since physical address has routing significance only withi ...

Keywords: MobileNAT, mobility

12 Design of a user-microprogrammable building block
Michael Kraley, Randall Rettberg, Philip Herman, Robert Bressler, Anthony Lake
November 1980 **Proceedings of the 13th annual workshop on Microprogramming**
Full text available: pdf(956.02 KB) Additional Information: full citation, abstract, references, citings, index terms

A user-microprogrammable computer has been developed for use as a building block in general-purpose and dedicated computer systems. The architecture is designed to be easily microprogrammed and features a 32-bit, vertically oriented microinstruction. The processor has a 135-nanosecond cycle time, either 16- or 20-bit macro data paths, and 1024 hardware registers. A significant fraction of the processor bandwidth may be budgeted for I/O processing to allow the substitution of microcode for e ...

13 Interactive Editing Systems: Part II
Norman Meyrowitz, Andries van Dam
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Full text available: pdf(9.17 MB) Additional Information: full citation, references, citings, index terms

14 Recovery blocks in action: A system supporting high reliability
T. Anderson, R. Kerr

October 1976 **Pr ceedings f the 2nd international c nference on Software engineering**

Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, references, citings, index terms

The need for reliable complex systems motivates the development of techniques by which acceptable service can be maintained, even in the presence of residual errors. Recovery blocks allow a software designer to include tests on the acceptability of the various phases of a system's operation, and to specify alternative actions should the acceptance tests fail. This approach relies on certain architectural features, ideally implemented in hardware, by which control and data structures can be ...

Keywords: Error detection, Error recovery, Recovery block, Recovery cache, Reliability, Software fault-tolerance

15 Kernel Korner: Device Drivers Concluded
August 1996 **Linux Journal**

Full text available: html(30.94 KB) Additional Information: full citation, index terms

16 File servers for network-based distributed systems
Liba Svobodova
December 1984 **ACM Computing Surveys (CSUR)**, Volume 16 Issue 4

Full text available: pdf(4.23 MB) Additional Information: full citation, references, citings, index terms, review

17 Integrating segmentation and paging protection for safe, efficient and transparent software extensions
Tzi-cker Chiueh, Ganesh Venkitachalam, Prashant Pradhan
December 1999 **ACM SIGOPS Operating Systems Review , Proceedings of the seventeenth ACM symposium on Operating systems principles**, Volume 33 Issue 5

Full text available: pdf(1.54 MB) Additional Information: full citation, abstract, references, citings, index terms

The trend towards extensible software architectures and component-based software development demands safe, efficient, and easy-to-use extension mechanisms to enforce protection boundaries among software modules residing in the same address space. This paper describes the design, implementation, and evaluation of a novel intra-address space protection mechanism called *Palladium,* which exploits the segmentation and paging hardware in the Intel X86 architecture and efficiently supports safe ...

18 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection
B. R. Borgerson, M. L. Hanson, P. A. Hartley
January 1978 **Communications of the ACM**, Volume 21 Issue 1

Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, citings, index terms

The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture Is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System ...

Keywords: 1100 computer series, computer architecture, data management systems, end user facilities, executive control software, multiprocessing, multiprogramming, operating system, programming languages

19 Hardware support for fast capability-based addressing

Nicholas P. Carter, Stephen W. Keckler, William J. Dally

November 1994 **Proceedings of the sixth international c nference on Architectural support f r programming languages and perating systems**, Volume 29 , 28 Issue 11 , 5

Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, references, citings, index terms

Traditional methods of providing protection in memory systems do so at the cost of increased context switch time and/or increased storage to record access permissions for processes. With the advent of computers that supported cycle-by-cycle multithreading, protection schemes that increase the time to perform a context switch are unacceptable, but protecting unrelated processes from each other is still necessary if such machines are to be used in non-trusting environments.This pap ...

20 Special issue on persistent object systems: Adaptable pointer swizzling strategies in object bases: design, realization, and quantitative analysis

Alfons Kemper, Donald Kossmann

July 1995 **The VLDB Journal — The International Journal on Very Large Data Bases**, Volume 4 Issue 3

Full text available: pdf(2.69 MB) Additional Information: full citation, abstract, references, citings

In this article, different techniques for *"pointer swizzling"* are classified and evaluated for optimizing the access to main-memory resident persistent objects. To speed up the access along inter-object references, the persistent pointers in the form of unique object identifiers (OIDs) are transformed (swizzled) into main-memory pointers (addresses). Pointer swizzling techniques can be divided into two classes: (1) those that allow replacement of swizzled objects from the buffer before th ...

Keywords: object-oriented database systems, performance evaluation, pointer swizzling

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